REPORT NO. P66-27
HAC REF. NO. A6720-001

NON DISSIPATIVE SOLAR ARRAY OPTIMUM CHARGE REGULATOR

SECOND QUARTERLY REPORT

FEBRUARY 1966

AEROSPACE GROUP

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

NON DISSIPATIVE SOLAR ARRAY OPTIMUM CHARGE REGULATOR

CONTRACT NO. NAS5-9210

SECOND QUARTERLY REPORT

P66-27

FEBRUARY 1966

Research and Development Division

AEROSPACE GROUP

HUGHES AIRCRAFT COMPANY, CULVER CITY, CALIFORNIA

TABLE OF CONTENTS

ILLUSTRATIONS

1.0 SUMMARY OF EFFORT DURING THE SECOND QUARTER

This report summarizes the progress during the second quarter in the study and design of optimum power transfer circuits which are capable of coupling a spacecraft solar array to a battery. During this quarter, design and testing of the 50 watt regulator was begun.

Design and construction was performed on a functional circuit block level in order to facilitate optimization of each individual circuit function. A preliminary integration of the individual circuit blocks was performed and closed loop operation was achieved.

Since the need for solar panel simulation is a necessity in the checkout of both cases of optimum charge regulators, a portion of the last quarter's effort was spent in designing and fabricating a simulator. This simulator gives a variety of output characteristics for both the 50 watt and 250 watt cases. This flexibility is necessary so that all regulator designs can be tested under all conditions of input power. Along with the solar panel simulator, a battery simulator was also designed and constructed. This unit provides a constant voltage load over the entire design range of 12 volts to 45 volts and can handle over 250 watts of input power.

Three types of batteries were purchased and evaluation of these types will be made during the third quarter. The types procured were silver cadmium, silver zinc, and nickel cadmium.

Except for the design of the 250 watt regulator, all of the goals as outlined for this quarter, in the first quarterly report, were attained. The design was not undertaken during this period because it was felt that more information about the general circuit operation should be obtained before any further design was accomplished.

2.0 PROJECTION OF WORK TO BE ACCOMPLISHED

During the next two quarters, design and testing of the 50 watt regulator will be completed. Based on the information gained from this unit, design, construction and testing of a 2 phase 250 watt OCR will be performed. This phase of the program will be completed with the integration of the breadboards with the batteries.

2.1 PROPOSED SCHEDULE

The following is a schedule for the circuit design for the third quarter of the program.

a. Complete the circuit design for 50 watt regulator (Case I).
b. Perform the circuit design for 250 watt, 2ϕ regulator (Case II).
c. Complete all breadboard testing.
d. Perform breadboard environmental tests.
e. Evaluate batteries for both Case I and Case II.

3.0 TECHNICAL DISCUSSION

3.1 50 WATT OPTIMUM CHARGE REGULATOR

The design of the circuitry for the 50 watt OCR followed the basic guidelines as set down in the first quarterly report. However, some circuit modifications were made wherever it was necessary. The basic specifications for this regulator are shown in Table I.

The function of the optimum charge regulator is to monitor the output performance and to couple the maximum power into the battery. Since the voltage of the battery is relatively constant, the output current will be a measure of the output power.

The block diagram of the OCR is shown in Figure 3-1. In the optimum mode of operation, the current is sensed for the maximum average value. When it drops below the maximum by a preset amount, a signal is sent to modify the duty cycle of the switching circuit in order to cause the current to begin increasing again.

The circuit design and construction was based on the philosophy of individual functional blocks so that each could be optimized separately before final integration. The circuit blocks were divided into the grouping that follows:

(1) Switching circuit
(2) Duty factor modulator
(3) Bistable and integrator
(4) Peak holding comparator
(5) Current sensing amplifier

Solar Panel Characteristics		Battery Characteristics	
Open Circuit Voltage at 30°C	Rated Power	Voltage Range	Probable Type
21-30 V	35-50W	12-~~25~~ 20 V	Silver Cadmium or Silver Zinc

Table I. Summary of electrical characteristics.

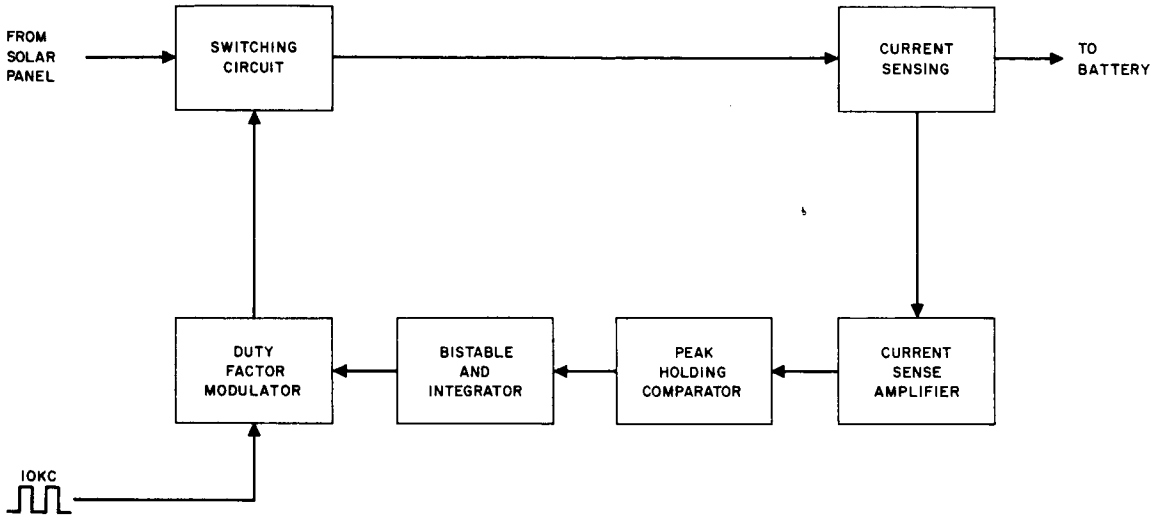


Figure 3-1. Optimum charge regular block diagram.

3.1.1 Switching Circuit

From an efficiency standpoint, the switching circuit is the most important functional block in the unit. This is evident from the fact that this circuit is directly responsible for the transfer of the solar panel energy to the battery.

Figure 3-2 is a generalized schematic diagram of the type of switching circuit which is being explored. As described in the first quarterly report, the basic energy transfer is accomplished by Q1 and L2. During the "on" time of Q1, the current I_1 is a linearly increasing ramp as shown by the photograph of Figure 3-3. This current along with current I_2 is shown in their relationships to V_{CE} (Q1) and each other. When Q_1 turns "off", the energy stored in L_2 is allowed to discharge into the battery through CR1. This current, I_2, is a linearly decreasing ramp.

3.1.1.1 Circuit Operation. When a positive voltage is present at the duty factor modulator (DFM) input, Q_5 is turned "on". This turns

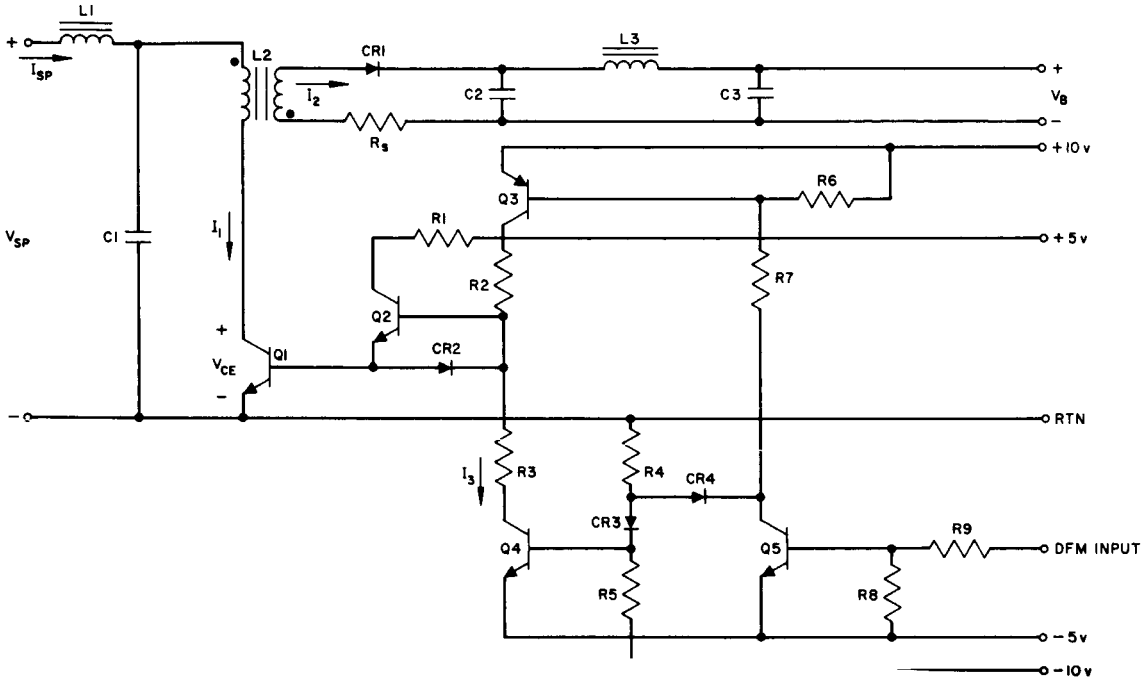


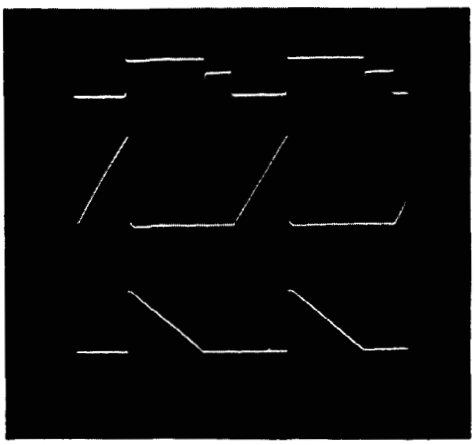
Figure 3-2. Generalized 50 watt switching circuit.

"off" Q_4, and turns "on" Q_3, Q_2 and finally Q_1. When this input drops to -5 volts, Q_5 is turned "off", thereby allowing Q_4 to turn "on" and back bias Q_1.

The conversion efficiency of this circuit can be found from computing the losses incurred by each component. Assuming Vsp = 25 volt, Isp = 2 amperes, and I_1 peak = 12 amperes (see Figure 3-3) then

$$D_1 = \frac{2 \times I_{sp}}{I_1 \text{ peak}} = .33$$

where D_1 is the duty cycle of Q_1.



(a) V_{CE} (Q_1) - 20v/cm

(b) I_1 - 4A/cm

(c) I_2 - 4A/cm

Horizontal: 20 μsec/cm

Figure 3-3. Switching circuit waveforms.

Table II lists each dissipation area, the equation defining each loss, and typical wattage losses.

In general, the dissipation in a resistor R due to a ramp of current is given by the relationship:

$$\text{Power} = R\left[\frac{1}{T}\int_{o}^{DT}\left(\frac{Ip\,t}{D\,T}\right)^2 dt\right] = \frac{RI_p^{\,2}\,D}{3} \qquad (1)$$

where

T = period of oscillation

D = duty cycle of current ramp

I_p = peak of current ramp

The total dissipation as shown in Table II represents that of the switching circuit losses. Adding the losses contributed by all of the other circuits brings the total to about 7.5 watts. This represents a total circuit efficiency of 85 percent. This is less than the desired

Dissipation Area	Defining Equation	Typical Loss
Q_1		
(a) Saturation	Equation 1 (R = R sat, D = D_1)	0.8 watt
(b) Switching	$\frac{I_1 \text{ peak}}{2} \frac{V \text{ peak}}{2} \times t_1 \times \frac{1}{T}$	1.0 watt
L_1	$I_{sp}^2 \times R_{L_1}$	0.2 watt
L_2	Equation 1 (R = R primary + R secondary, D = $D_1 + D_2$)	0.2 watt
CR1	Equation 1 (R = R_f, D = D_2)	0.8 watt
R_s	Equation 1 (R = R_s, D = D_2)	0.8 watt
L_3	$\left(I_{battery}\right)^2 \times R_{L_3}$	0.2 watt
Base Drive for Q_1		
(a) Turn "on" drive	$5V \times \frac{I_1 \text{ peak}}{10} \times D_1$	2.0 watts
(b) Turn "off" drive	$5V \times I_3 \times t_2 \times \frac{1}{T}$	0.2 watt
	TOTAL	6.2 watts

Note: t_1 = turn off time of Q_1

t_2 = turn off time of Q_2

Table II. 50 Watt switching circuit conversion losses.

efficiency of 90 percent and further investigation will be made into the areas where it is felt improvement is possible.

3.1.2 Duty Factor Modulator

As its name implies, this circuit generates a square wave whose duty cycle is a function of the crossover point between inputs V_1 and V_2 (see Figure 3-4). V_1 is a 10 kc triangular wave. This input is generated from a square wave which is integrated by Q_1 and Q_2 and their associated circuitry. V_2 is also a triangular wave but at the hunting frequency.

If V_1 has zero average value, then a 50 percent duty cycle will result if $V_2 = 0$. Similarly, if $V_2 = \pm V_1$ (peak), then a 0 percent or 100 percent duty cycle will result. Therefore, it can be seen that V_2

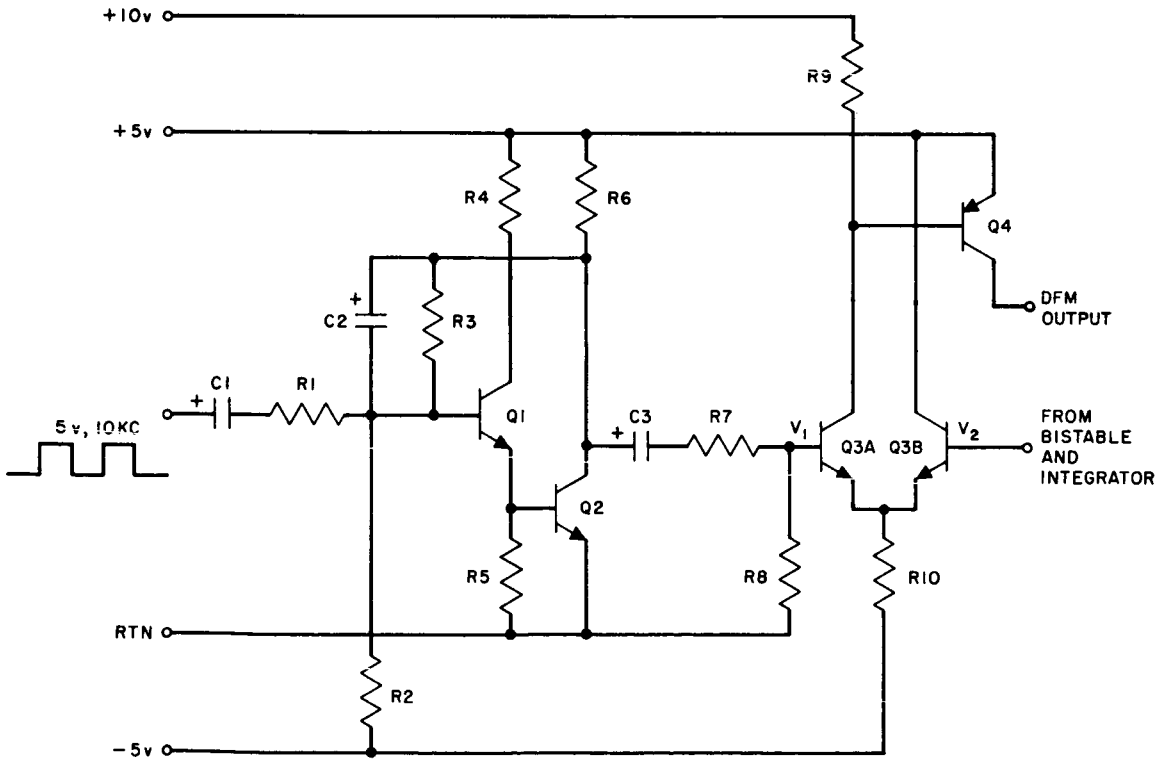


Figure 3-4. Duty factor modulator.

p-p must be very much less than V_1 p-p in order to keep the duty cycle variation to a minimum. This is necessary since the hunting zone and the hunting losses are directly proportional to the peak duty factor variations.

3.1.3 Bistable and Integrator

This circuit converts the pulses which are generated by the peak holding comparator to a square wave that is integrated to obtain a triangular wave. This output triangle is used to control the duty factor modulator. Figure 3-5 is a schematic diagram of a circuit which is being considered to perform this function.

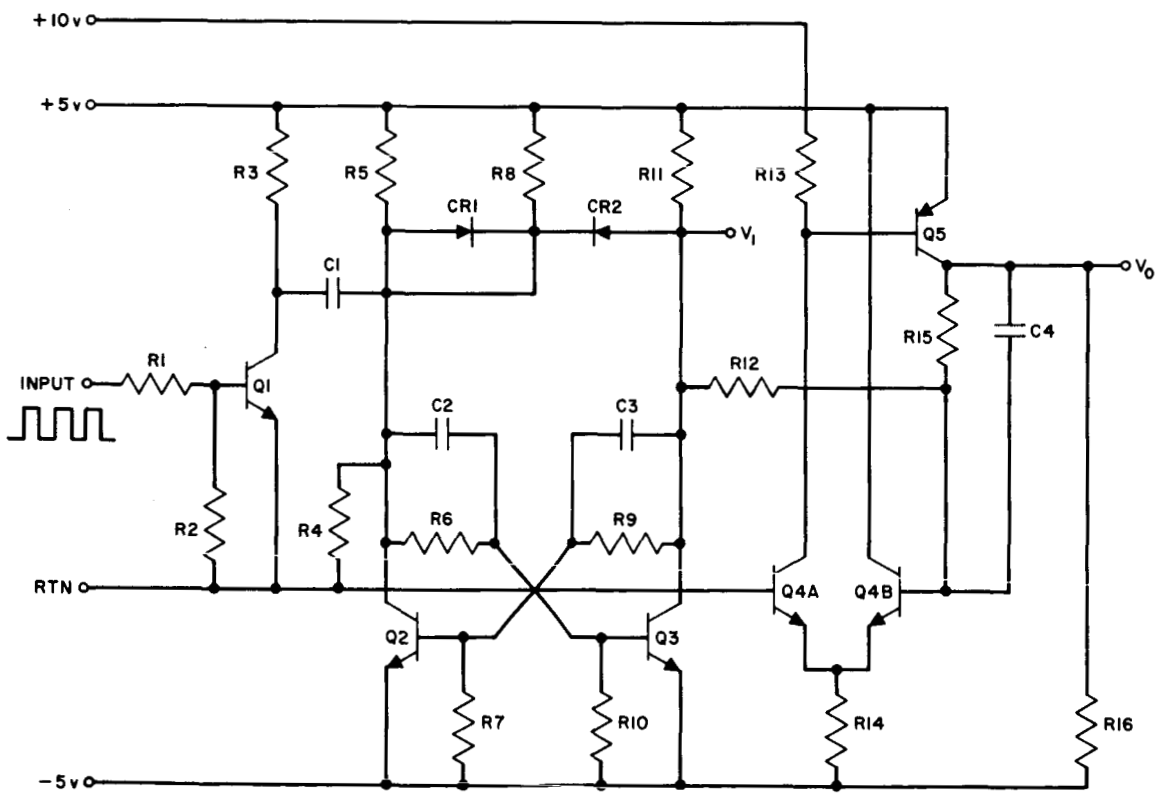


Figure 3-5. Bistable and integrator.

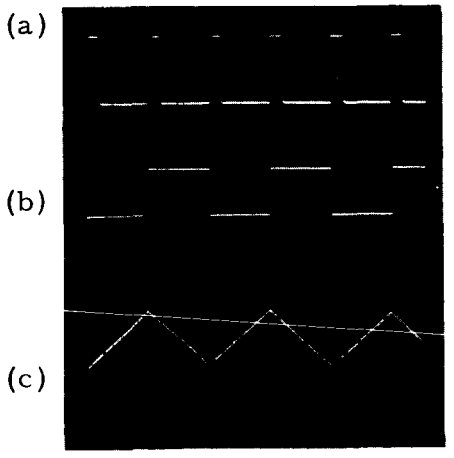
Transistor Q_1 inverts the incoming positive pulses which are then used to trigger the bistable formed by Q_2 and Q_3. The resultant square wave is then integrated by the circuit associated with Q_4 and Q_5.

Some of the waveforms associated with this circuit are seen in Figure 3-6.

3.1.4 Peak Holding Comparator

This circuit compares the maximum value of its input, Vin, to the instantaneous value of Vin. When the instantaneous value falls a preset amount below the maximum value, a pulse is generated which is then used to control the bistable.

Figure 3-7 is a schematic diagram of a circuit under consideration. As Vin increases, the voltage (V_2) across C_1 increases at the same rate as V_1. When Vin begins decreasing, thereby causing V_1 to decrease, V_2 remains constant at the peak value of Vin because of the



(a) Input - 5v/cm

(b) V_1 - 5v/cm

(c) V_0 - 50μv/cm

Horizontal: 1 msec/cm

Figure 3-6. Bistable and integrator waveforms.

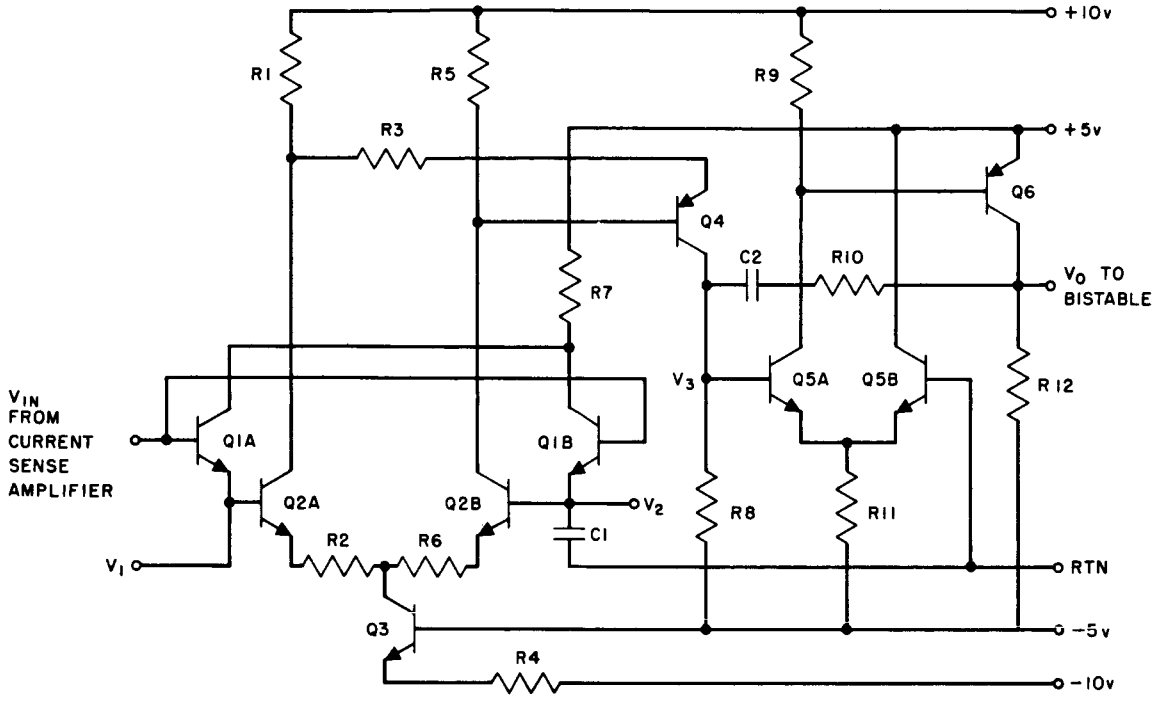


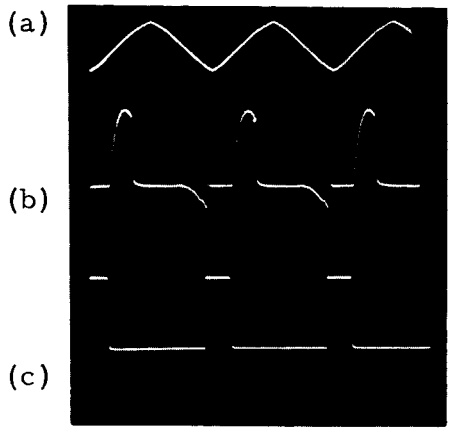
Figure 3-7. Peak holding comparator.

charge stored on C_1. This difference voltage (V_1 - V_2) is then amplified by Q_2 and Q_3, and V_3 is produced. When $V_3 \cong 0$, Q_6 is turned on which permits Vo to go from -5V to +5V. Current is also fed back through R10 and C2 to cause Q5 and Q6 to regenerate "on" until the time when C2 charges up. At this time, Vo drops back to -5 volts and the cycle begins anew.

Figure 3-8 shows some typical wave forms which are generated by this circuit. The input (Figure 3-8 (a)) is a 500 cps triangular wave that simulates the average current variations.

3.1.5 Current Sense Amplifier

The current sense amplifier, as shown in Figure 3-9, amplifies the average current variations to a level, which is useful to the peak



(a) V_{IN} - 2V/cm

(b) $V_1 - V_2$ - .5V/cm

(c) Vo - 5V/cm

Horizontal - 0.5 msec/cm

Figure 3-8. Peak holding comparator waveforms.

holding comparator. It also acts as a filter to eliminate the 10 kc variations in the current waveform.

3.2 SOLAR PANEL SIMULATOR

Figure 3-10 is a block diagram of the solar panel simulator. Basically it consists of a linear regulator whose output voltage is a function of the current being drawn. This control is accomplished by varying the regulator's reference voltage as a function of output current.

An SCR switching preregulator provides the input voltage to the linear regulator. This circuit maintains the linear regulator input +10 volts above the output voltage. Dissipation in the main pass stages is limited in this manner.

A dc/dc converter provides the bias voltages for the operation of the various circuits in this unit. A +60 volt DC source is also provided for operation of the battery simulator.

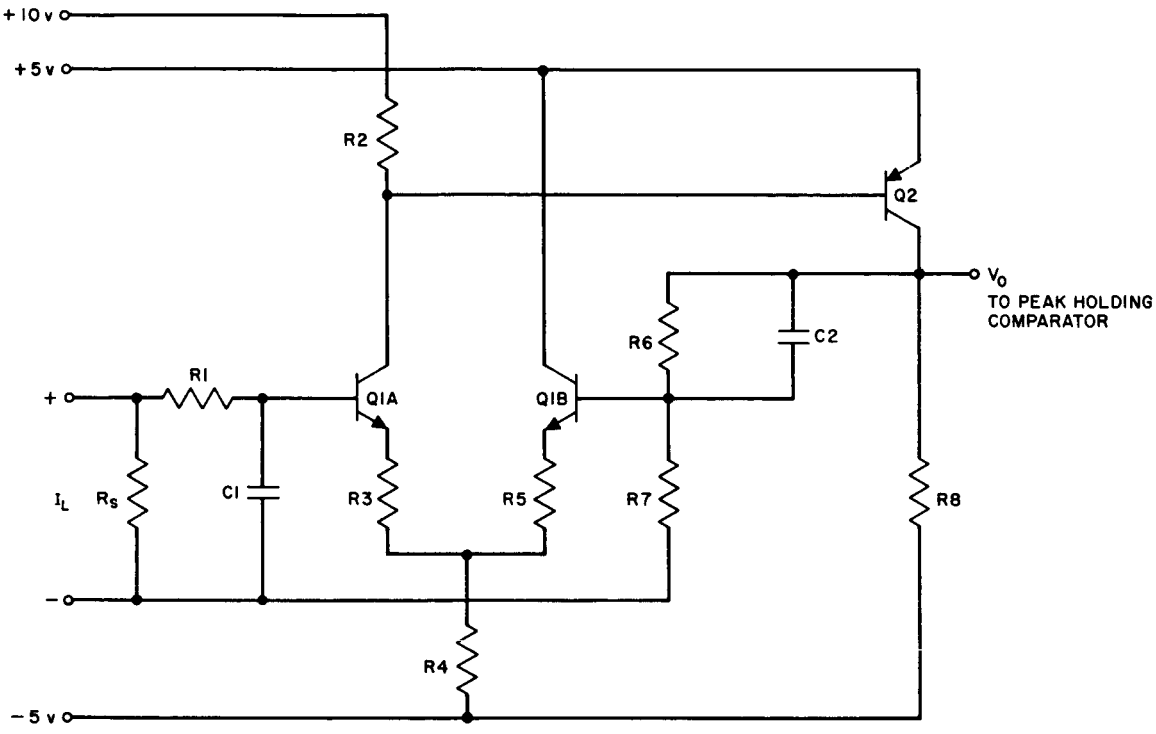


Figure 3-9. Current sense amplifier.

The solar panel simulator is capable of supplying 10 amperes at 60 volts dc continuously. It has built-in current limiting, which is adjustable from 0 to 10 amperes.

The output characteristics are capable of adjustment through a wide range. For simulated temperature variations the open circuit voltage is continuously adjustable from 0 to 60 volts. Figure 3-11 (a) shows some typical output characteristics and their variation due to simulated temperature changes.

The variations due to simulated illumination changes range from a few hundred milliamperes short circuit current to 10 amperes. Figure 3-11 (b) shows some typical output characteristics and the variations due to illumination.

Degradation controls are also provided in order to allow complete freedom to shape the simulator characteristics. Figure 3-11 (c)

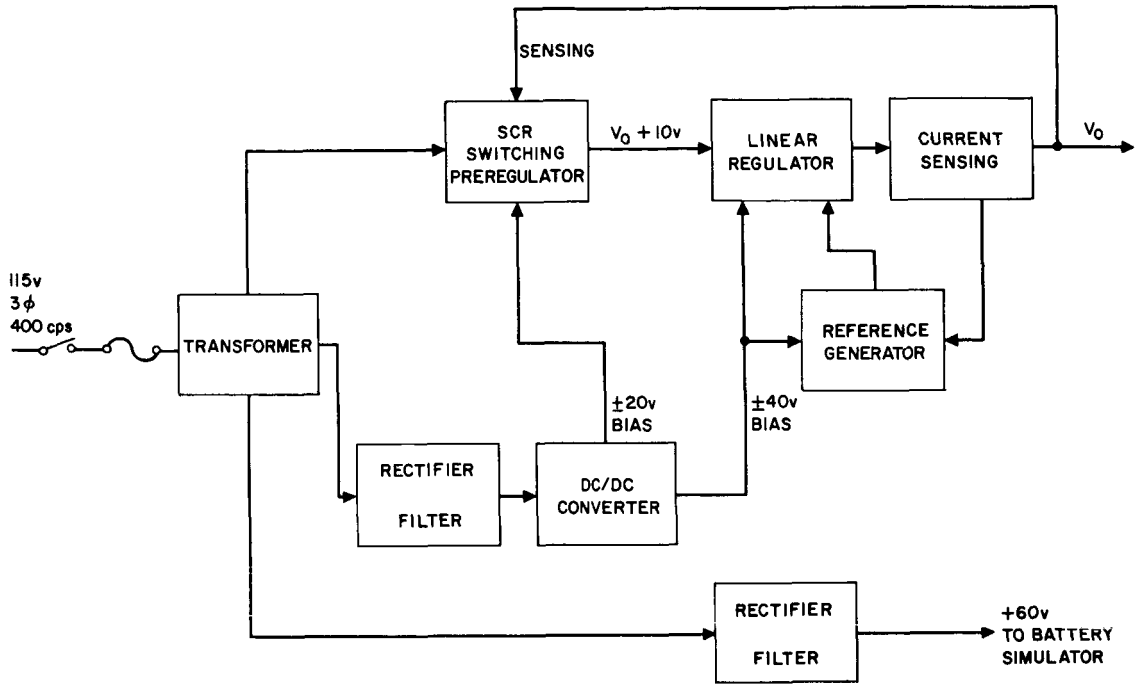


Figure 3-10. Solar panel simulator block diagram.

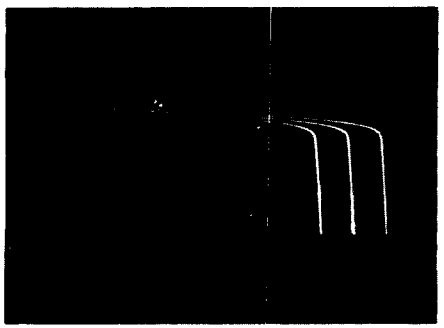
shows some of the characteristics available with the manipulation of these controls.

A photograph of the breadboard model of this unit is shown in Figure 3-12.

3.3 BATTERY SIMULATOR

The battery simulator simply consists of a shunt regulator whose regulation voltage is variable from 12 to 45 volts. It has two operating modes. The first is the 12 to 25 volts range and it is capable of dissipating 125 watts in this mode. The second is the 25 to 45 volts range. In this mode it can dissipate 250 watts.

Figure 3-13 shows a picture of this unit.



(a) Variations due to temperature

(b) Variations due to illumination

(c) Variations due to degradation

Vertical - Io: 2.5A/cm

Horizontal - Vo: 6V/cm

Figure 3-11. Typical characteristics available from the solar panel simulator.

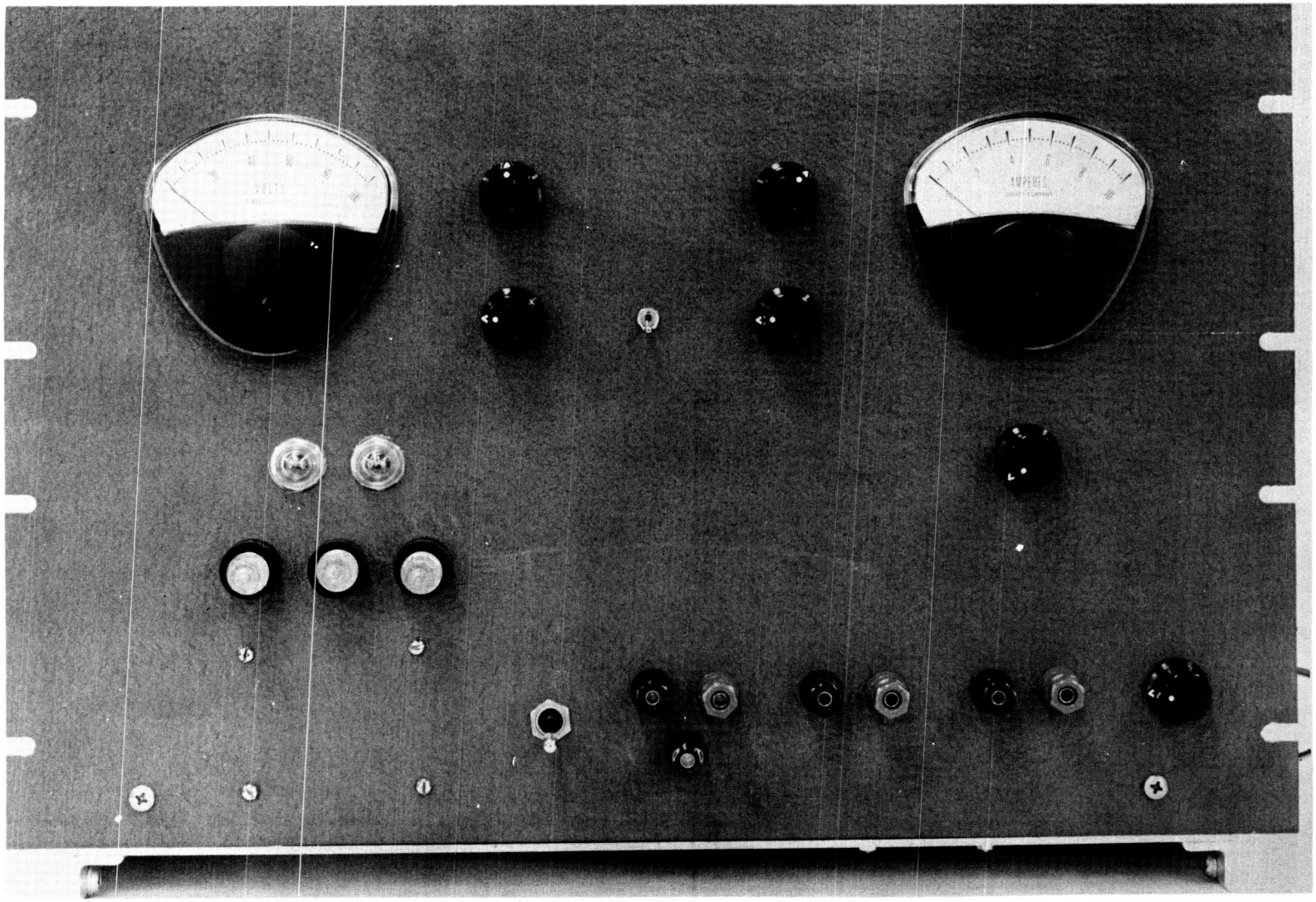


Figure 3-12. Breadboard model of the solar panel simulator.

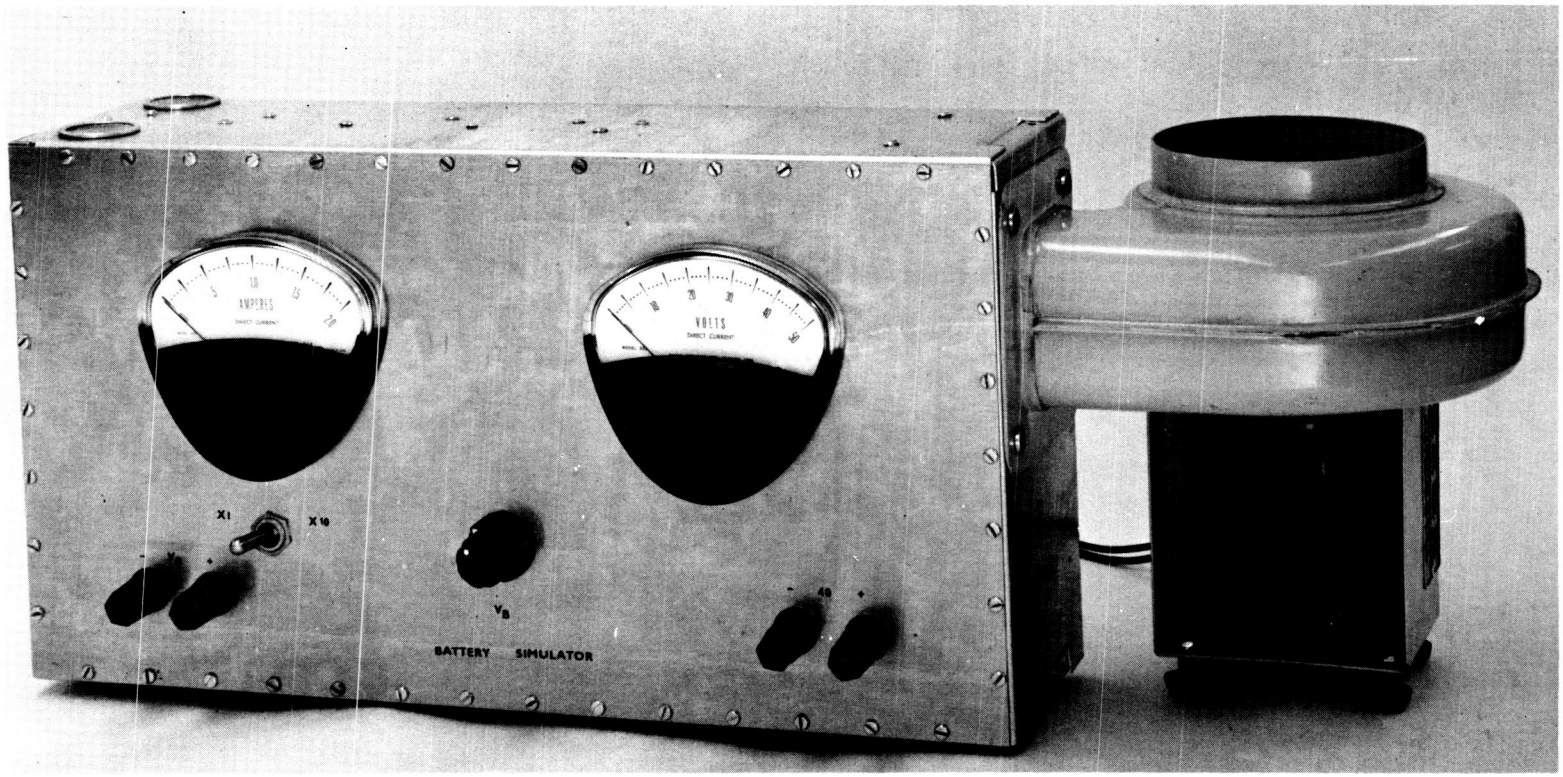


Figure 3-13. Battery simulator.